

Carinthia University of Applied Sciences

Systems Design / Systems Engineering

**Report for Module 5&6**

“Data Acquisition and Transmission”

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| Grade: |  |

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# Delta – Sigma ADC

First task requires students to setup a fist order delta – sigma ADC loop in Simulink with following values:

* 100 kHz sampling frequency
* FS range +/- 5 V
* %0 Hz +/-2 V sinusoidal signal at the input

Following Simulink was proposed:

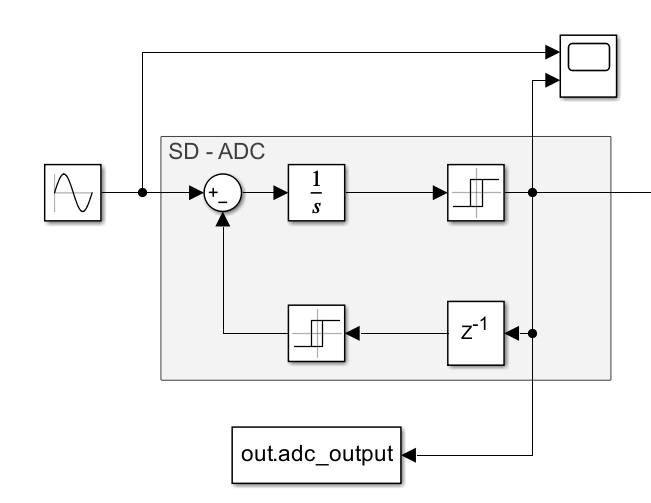


Figure 1: Proposed Simulink model for first task

The parameters for blocks are as follows:

Table 1: Block parameters for Simulink Model on Figure 1

|  |  |
| --- | --- |
| Integrator | Default settings |
| Switch-on/off point for forward path relay | 0 |
| Output when on/off | On: 1, Off:-1 |
| Sampling time for delay block | 10e-5 kHz |
| Delay order | 1 |
| Switch-on/off point for feedback path relay | 0 |
| Output when on/off | On: 5, Off:-5 |

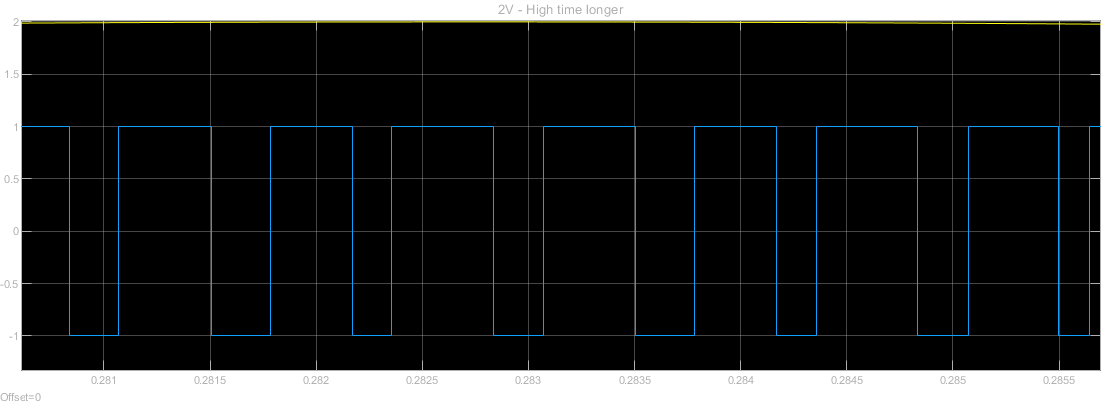
Output for this ADC is as follows:

Figure 2: ADC output around +2V input

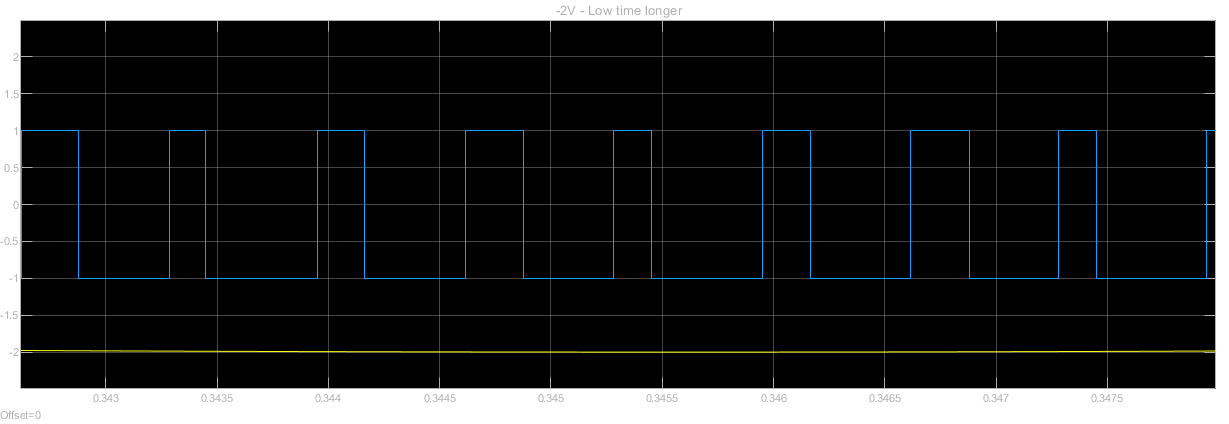
The output of the ADC near +2V input demonstrates higher on time than low time. This situation is reversed near –2V, as seen on the following figure.

Figure 3: ADC output near -2V input

# Digital Filtering

On the second part, a comb filter with 4 different decimation factors were employed to show the effects of sampling rate reduction. Following model was setup for the task:

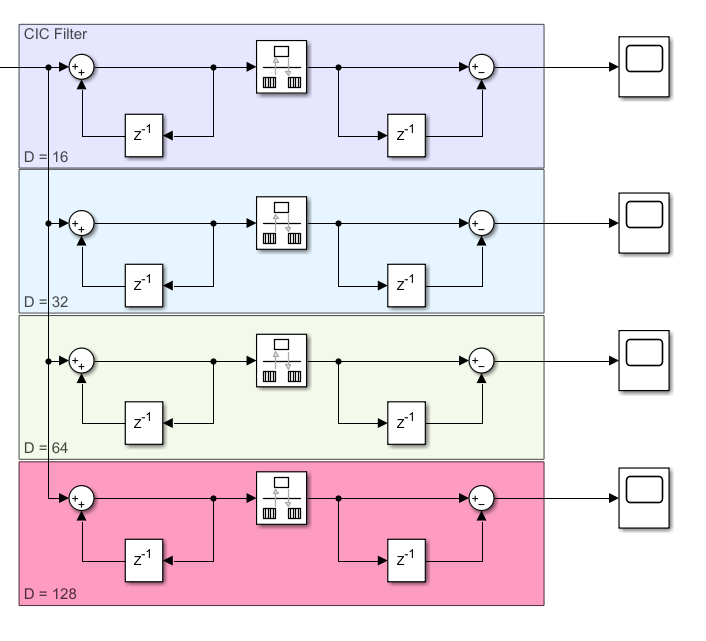


Figure 4: CIC filter with decimation

The following parameters were used for blocks:

Table 2: Block parameters for Simulink Model on Figure 4

|  |  |  |
| --- | --- | --- |
| Decomation Factor | Delay Blocks Sample Time | Rate Transition Sample Time |
| 16 | 16\*10e-5 Khz | |
| 32 | 32\*10e-5 Khz | |
| 64 | 64\*10e-5 Khz | |
| 128 | 128\*10e-5 Khz | |

The corresponding outputs of decimation filters are as follows:

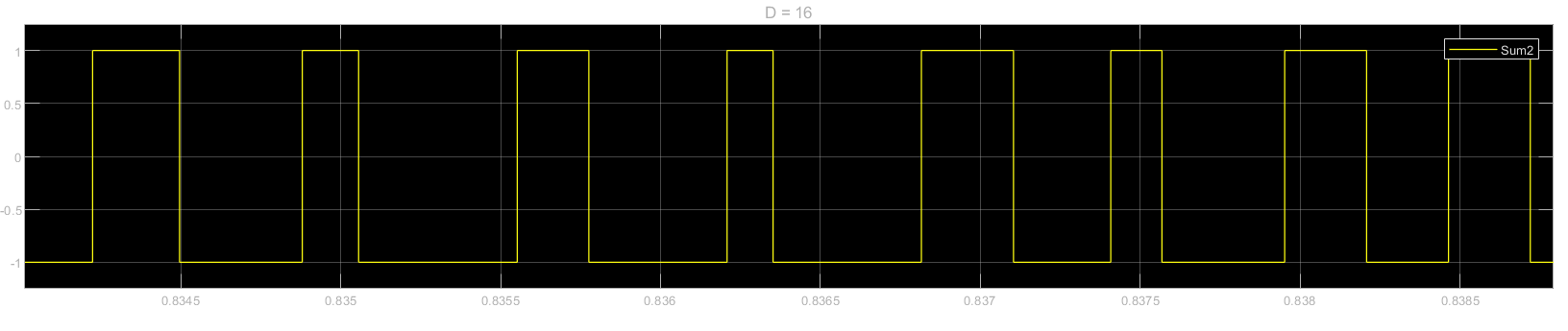


Figure 5: D = 16

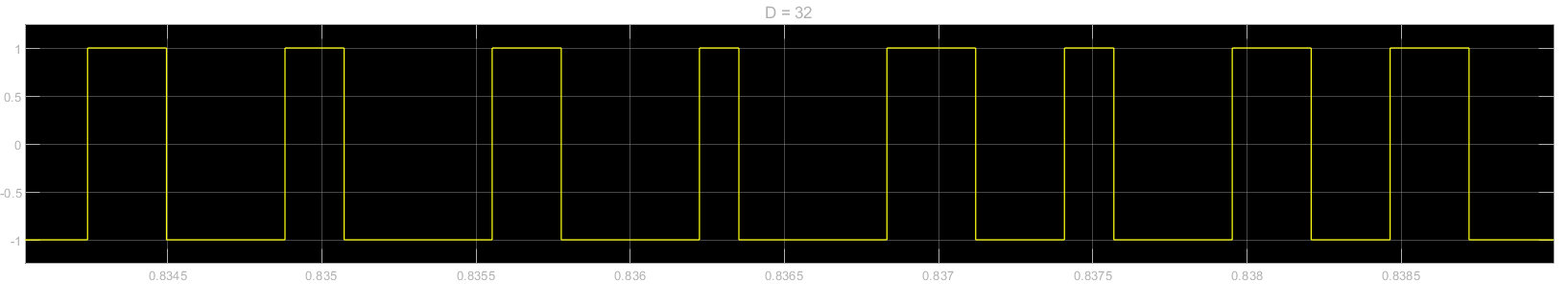


Figure 6: D = 32

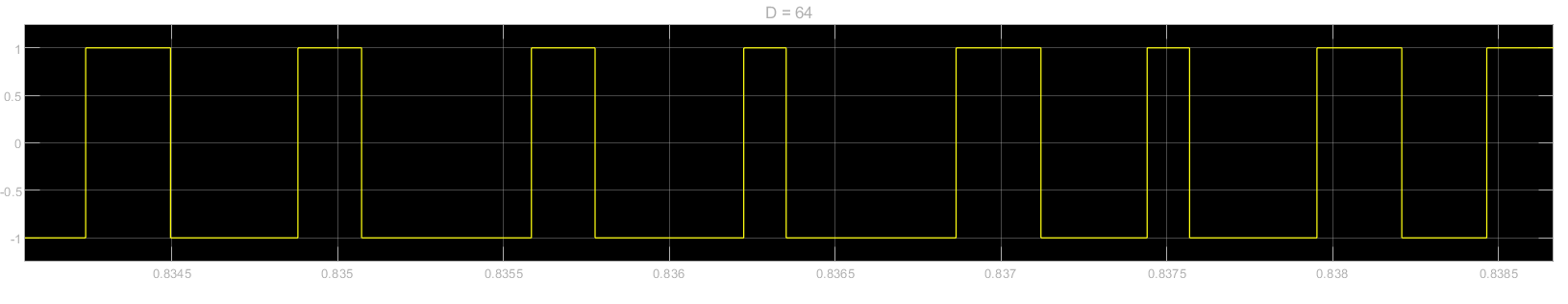


Figure 7: D = 64

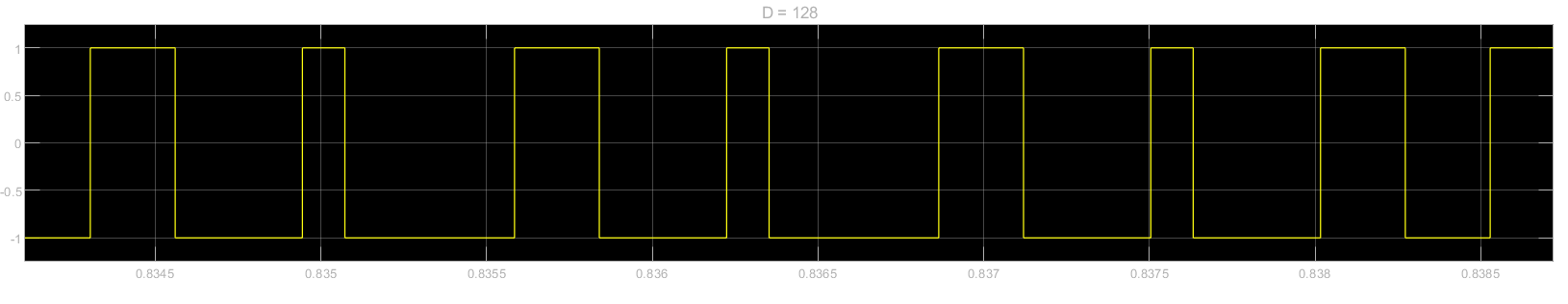


Figure 8: D = 128

The snippets shown above cover 4 millisecond window between 0.8345 – 0.8385 seconds. Even though the decimation factors differ by factor of 2, outputs look similar. The reason is unknown for student.

# Signal Transmission Rate

Calculate the estimated maximum digital data rate for the following interface SPI system:

* An SPI output driver with Rout = 50 Ω
* Serial resistor RS = 470 Ω for shortcut protection
* A wiring harness with ESD blocking capacitance CW =150 pF
* Pad capacitance to ground CPAD =5 pF each

**Fixed Point Implementation Examples:**

X = 4.375 in u4.4

Y = -3.25 in s4.4

X2 (define yourself the result representation) → **u8.8**

X = 0 1 0 0 0 1 1 0 = 0.23 + 1.22 + 0.21 + 0.20 + 0.2-1 + 1.2-2 + 1.2-3 + 0.2-4

Y = 1 1 0 0 1 1 0 0 = 1.-23 + 1.22 + 0.21 + 0.20 + 1.2-1 + 1.2-2 + 0.2-3 + 0.2-4

X2= 19.1406 = 0 0 0 1 0 0 1 1 0 0 1 0 0 1 0 0 = 24 + 21 + 20 + 2-3 + 2-6